REMARKS

Claims 1-10 and 14-21 are pending. No amendments are being submitted.

In section 7 of the Office Action, Claims 1, 2 and 5 are rejected under 35 USC § 102(b) as being anticipated by US patent No. 5,996,057 (hereinafter referred to as "the Scales, III et al. patent"). Applicants are traversing this rejection.

The application contains three independent claims, namely Claims 1, 2 and 5. Below, Applicants explain that the Scales, III et al. patent does not disclose all of the elements of Claims 1, 2 and 5.

The general disclosure of the Scales, III et al. patent was discussed in Applicants' response to the previous Office Action. For the sake of ease of reference, according to col. 2, lines 60-66 of the Scales, III et al. patent, the data processing system allows the specification of 3 input operands comprising 2 input vectors and a control vector. The input operands are loaded into vector registers and a Permute-With- Replication (PWR) operation is performed on the 2 input vectors in a manner specified by the control vector. The result of the PWR operation is stored as an output operand in an output register.

Col. 5, lines 33-34 of the Scales, III et al. patent describes that the system disclosed therein comprises a vector register file 200 having 32 vector registers. The vector register file 200 is coupled to a combine network 210 (col. 5, lines 35-36). The vector register file 200 provide 3 vectors (A, B and C) from 3 pre-selected or programmed registers of the vector register file 200 (col. 5, lines 36-38). The PWR operation is performed by the combine network 210, and the vector register file 200 includes a control register containing the control vector (col. 5, lines 46-47).

Referring to FIG. 3 of the Scales, III et al. patent, col. 5, lines 43 – 48 states:

> "*FIG. 3 shows a block diagram of the four specific registers within vector registers 200 utilized to perform the PWR operations of the preferred embodiment. Vector registers 200 include control register 305 (VC) containing the control vector, input registers 310 (VA) and 315 (VB) and the output register 320 (VT).*" [Emphasis added]

In Sections 7 and 8 of the Office Action, reference is made to col. 2, line 59 to col. 3, line 13. In particular, reference is made in the Office Action to text within col. 3, lines 3 – 5:

> "*The control vector can be specified in the operational code or be the result of a computation previously performed within the vector registers.*" [Emphasis added]

Applicants understand that the reasoning set out in the present Office Action relies upon this passage on the basis that the above passage implicitly discloses some form of control means. However, the above passage relates to the specification of a vector. This is, it must be pointed out, distinct from the selection of a vector.

It is also noted that col. 8, lines 60 – 64 contains an analogous statement:

> "*The control vector register VC is loaded with a control vector designated by the operational code or computationally derived from a previous operation to implement a desired high-performance data processing function.*"

However, col. 8, line 64 to col. 9, line 2 continues by stating:

> "*Each of the input registers VA and VB are loaded with properly aligned data vectors to be processed. The data processing system of the present system then performs a PWR operation on the two input vectors VA, VB as a function of the control vector loaded in the control register VC.*" [Emphasis added]

Hence, Applicants understand the above passage as teaching that the control vector is pre-stored in the VC and is used to operate on the input registers VA and VB. Further, Applicants understand that the manner in which said control vector came to be in the VC is as a result of the "specification" described at col. 3, lines 3 – 5.

Claim 1 recites, *inter alia*, the following features:

- a permutation logic block coupled to receive and permutate vectors from at least one vector register according to control parameters;
- a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and
- a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

Whilst the Office Action suggests that the Scales, III et al. patent implicitly discloses a controller, the Scales, III et al. patent does not teach a controller that is coupled **between** the plurality of control registers and the permutation logic block as recited in Claim 1. Likewise, the Scales, III et al. patent does not disclose selection of one of the control registers by a controller as recited in Claim 1. Furthermore, the Scales, III et al. patent does not disclose that the **controller** provides the control parameters **from** the selected one of the plurality of control registers **to** the permutation block as recited in Claim 1.

With the greatest of respect to the observations set forth in the present Office Action, any suggestion that all of the above-mentioned features are implicitly disclosed by the text spanning col. 2, line 59 to col. 3, line 4 is an application of ex-post facto analysis and the MPEP is clear as to the avoidance of the use of such hindsight.

Furthermore, if it is contemplated to argue that the "specification" step identified in the present Office Action must, as a matter of necessity, be preceded by a selection stage performed by the (allegedly) implicitly disclosed controller, it is respectfully further pointed out that any such selection would not conform the features identified above that are specifically recited in Claim 1.

In view of the reasoning provided above, Applicants submit that the Scales, III et al. patent does not anticipate Claim 1.

Claims 3, 4, and 8-10 depend from Claim 1. By virtue of this dependence, Claims 3, 4 and 8-10 are also novel over the Scales, III et al. patent.

Claim 2 provides for a single-instruction multiple-data microprocessor vector permutation system comprising control means coupled between the plurality of control registers and the permutation logic block. As explained above in support of Claim 1, the Scales, III et al. patent does not disclose a controller coupled between the plurality of control registers and the permutation logic block, the selection of one of the control registers by a controller, nor that the controller provides the control parameters from the selected one of the plurality of control registers to the permutation block. Accordingly, the Scales, III et al. patent does not anticipate Claim 2.

In view of the reasoning provided above, Applicants submit that the Scales, III et al. patent does not anticipate Claim 2.

Claims 14-18 depend from Claim 2. By virtue of this dependence, Claims 14-18 are also novel over the Scales, III et al. patent.

Claim 5 provides for a method for permutation in a single-instruction multiple-data microprocessor where control means are provided between the plurality of control registers and the permutation logic block. As explained above in support of Claim 1, the Scales, III et al. patent does not disclose a controller coupled between the plurality of control registers and the permutation logic block, the selection of one of the control registers by a controller, nor that the controller provides the control parameters from the selected one of the plurality of control registers to the permutation block. Accordingly, the Scales, III et al. patent does not anticipate Claim 5.

In view of the reasoning provided above, Applicants submit that the Scales, III et al. patent does not anticipate Claim 5.

Claims 6, 7, and 19-21 depend from Claim 5. By virtue of this dependence, Claims 6, 7, and 19-21 are also novel over the Scales, III et al. patent.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Customer Number: 23125

By: /David G. Dolezal/
David G. Dolezal
Attorney of Record
Reg. No.: 41,711
Telephone: (512) 996-6839
Fax No.: (512) 996-6853